WIZNOVA

MMD1000

MAGNETIC STRIPE CARD READER IC

General

The MMD1000 chip integrates the magnetic card reader function with data encryption and has external device via universal asynchronous receiver and transmitter (UART) or serial peripheral interface (SPI). The chip supports up to 3 track card reading at the same time. Signal processing techniques are employed to recover F2F encoded data reliably from head signals with severe fluctuation of signal amplitude, widely varying bit interval, and jittery bit position. The recovered data is encrypted with the 128 bit AES.

Features

- Full three track support
- Signal conditioning adapted to head signal
- Digital signal processing for superior data recovery performance. (See Block Diagram)
- Encrypts all track data
- Secure data transfer with 128 bit AES encryption: CBC mode
- DUKPT key management (Derived Unique Key Per Transaction)
- ISO/IEC 7811 and binary data format support
- Flexible external interface: UART or SPI
- Wide range of card swipe speed : from 5 to 150 cm/s
- Minimum external components requirement. (See Recommended Circuit)

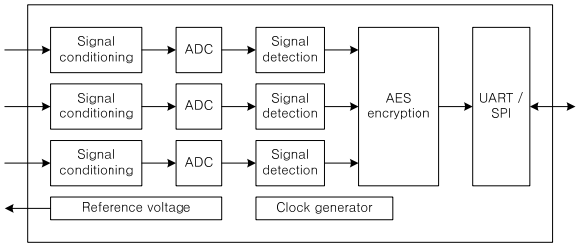
Application

- Point of Sale Terminal
- ATM Machine
- Card Key Entry System

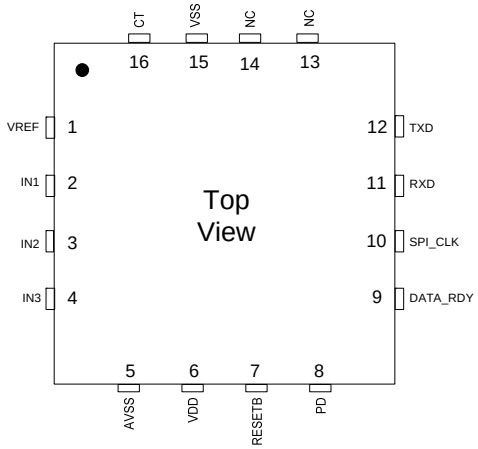
Description

The chip integrates the magnetic card reader function with data encryption. Upon reception of the magnetic head signals, the card data are recovered, encrypted, and transferred to the external device via universal asynchronous receiver and transmitter (UART) or serial peripheral interface (SPI). The chip supports up to 3 track card reading at the same time. Signal processing techniques are employed to recover F2F encoded data reliably from head signals with severe fluctuation of signal amplitude, widely varying bit interval, and jittery bit position. The recovered data is encrypted with the 128 bit AES. The figure below shows a simplified block diagram of the chip.

Block Diagram



Package: 4x4mm2 16QFN

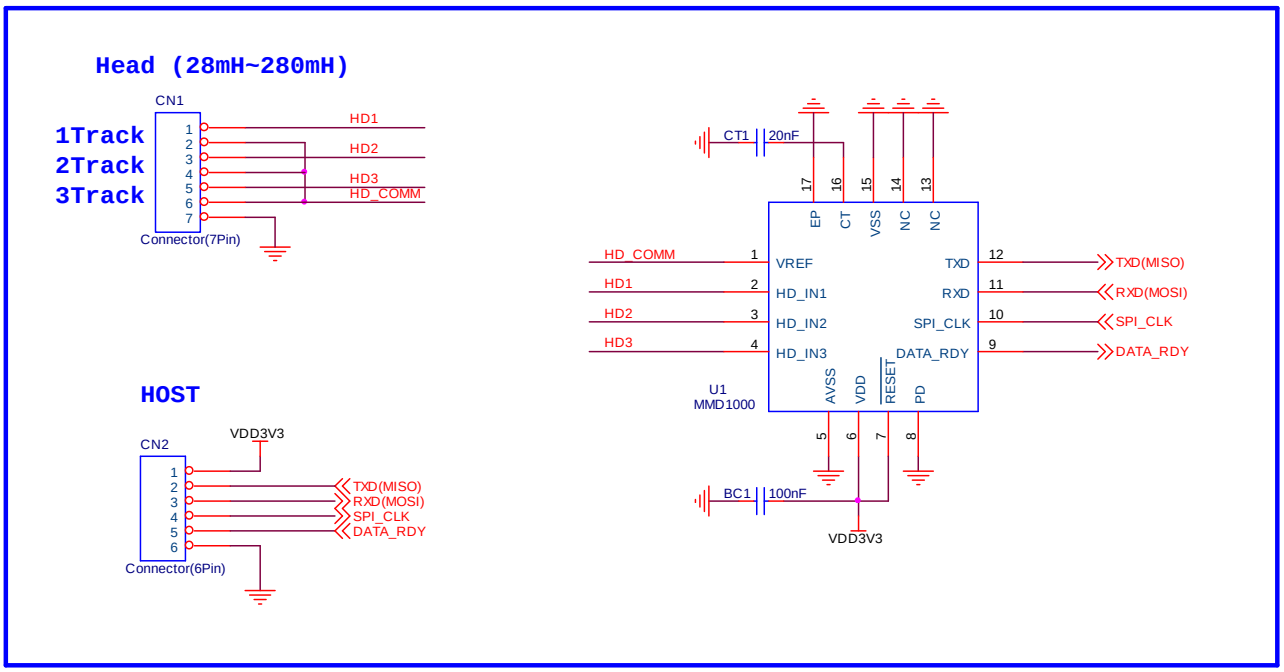


Pin Description

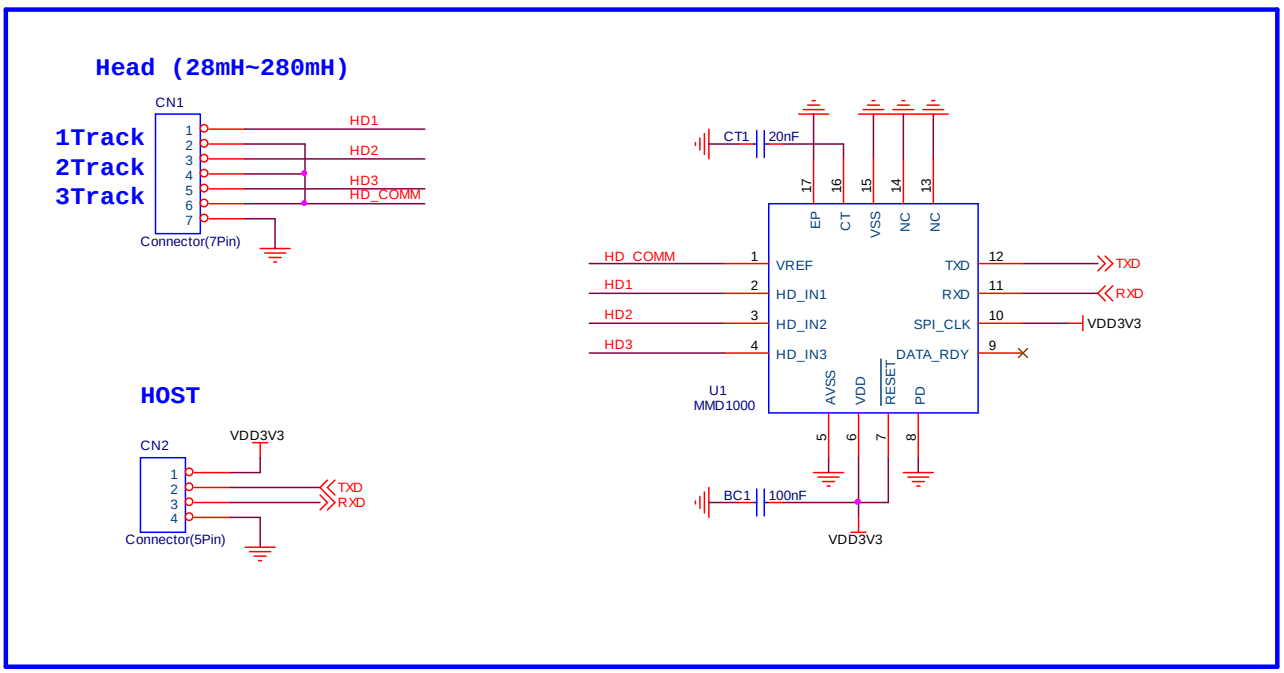
Pin name	Description
VREF	Reference voltage for head
IN1	Track 1 head signal
IN2	Track 2 head signal
IN3	Track 3 head signal
AVSS	Analog ground
VDD	Power supply (3.3V)
RESETB	External reset signal
PD	Power down
DATA_RDY	Data ready for SPI
SPI_CLK	SPI clock
RXD	UART/SPI receive data
TXD	UART/SPI transmit data
NC	Tie to the ground VSS
NC	Tie to the ground VSS
VSS	Digital ground
CT	External capacitor connect

Recommended Circuit

• SPI Mode Circuit



• UART Mode Circuit



WIZNOVA, Inc.
www.wiznova.com

403, Daedeok Plaza 1
12 , Dochon-ro, Jungwon-gu, Seongnam-si,
Gyeonggi-do, 462-080, South Korea
Tel +82-31-723-7714, Fax +82-31-723-7721
contact@wiznova.com